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Multiplexer Based Digital Integrated Circuit Tester

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Abstract: The basic function of the digital IC tester is to test digital IC for correct logical functioning as described in the truth table. It can test digital ICs having 14 pins. This model applies the necessary signals to the inputs of the IC, monitoring the outputs at each stage and comparing them with the outputs in the truth table. Any discrepancy in the functioning of the IC results in a fail indication through LEDs. The testing procedure is accomplished with the help of keys present on the main board. At this stage we had completed to test the most common used digital IC's used in our laboratories, mainly belonging to the 74TTL series. This tests various types of ICs like AND, OR, EX-OR, NAND, NOR and EX-NOR gates.

Key Words: Inequality detector, Multiplexer, Flip-flops, Socket and Counter.

I. INTRODUCTION

In any manufacturing industry there are continuous efforts in cost reductions, upgrade quality and improve overall efficiencies. In electronic industry, with dramatic increase in circuit complexity and the need for the higher levels of reliability, a major contributor cost in any product can be in the testing. However we should recognize in the real world that no product is perfect, so that testing and in particular automatic testing will be an essential part of production in the foreseeable future. In industries, research centers and college, some common IC's are frequently used; many times people face problems due to some fault in these integrated circuits. So it is very essential to test them before actually using them in any of the applications. Digital IC tester is best solution for these problems. This project has the capability of testing digital IC's like AND, OR, EX-OR, NAND, NOR and EX-NOR gates of 14 pins.

The IC-tester tests the basic logic gates used in the digital laboratory of colleges. The input is given to the corresponding pins of the IC to be tested using Mod-4 synchronous up counter (Input generator). The output is taken from the relevant pin. It is compared with the output generated by output generator. The output generator comprises of combinational logic design according to the truth table given in Table 1. Depending on the result of comparison, using inequality detector, the output is indicated through LEDs.

II. MOTIVATION

The digital IC tester is implemented in order to test the digital IC's to verify the faulty gates and the good gates. The necessary inputs to the gates of the IC to be tested which is placed in the test socket and corresponding outputs are accumulated and sent to the inequality detector where the output is compared with the logic table and if any discrepancy results, it displays the fail through LEDs. The primary purpose of this digital IC tester is that it can easily check the IC within due course of time and if any discrepancy results then it determines the gates which were good ones and which were the bad ones. The manual operation or a human intervention includes testing of each individual IC by making necessary connections and verifying the outputs for each gate by the truth table is a time taking and tedious process. With the implementation of the output generator (multiplexer) it makes the job much easier to receive data for the respective gates and process output and display results.

III. BLOCK DIAGRAM

This model consists of five main blocks: clock generator, mod-4 asynchronous counter, output- generator, test socket and inequality detector. The Block diagram of digital IC tester is shown in Fig. 1.

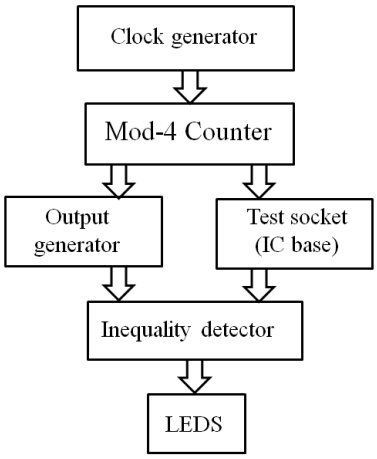

Fig. 1: Block diagram of digital IC tester

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IV. DESCRIPTION

A. DC power supply unit

A regulated 5 volt DC supply is essential for powering this circuit. The output of most wall-warts and adapters is to rippled and impure for use in digital circuits. So building an inexpensive power supply using some discrete components and a fixed voltage regulator IC is better.

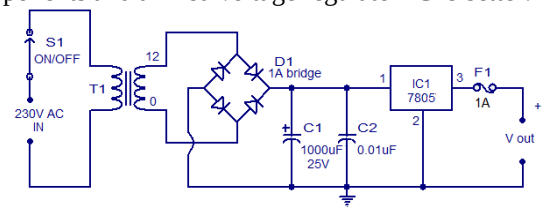

Fig. 2: Rectifier using capacitive filter

The circuit consists of three main blocks, the rectifier, filter and regulator. The rectifier is used to transform the mains AC voltage to a suitable DC voltage. The output of the rectifier is however an impure DC signal so we use a filter to clean the signal and finally a regulator to deliver precisely 5 volts, irrespective of the load connected to the output.

1) Rectifier: It consists of a transformer and a diode bridge. The diodes are standard silicon 1N4007 diodes. Instead of diodes, we have used "D2SB" – RECTIFIER. We have chosen a 12V transformer because the regulator IC needs at-least 7.5V of input voltage to function properly.
2) Filter: The capacitive filter is used here. The capacitive filters are great for light load applications like digital circuits
3) Regulator: The voltage is regulated by three terminal voltage regulator IC – LM7805. This regulator provides stable 5V DC output against large fluctuations in input voltage and load. It also has internal protection circuits which 'brownout' the device when overloaded. To decide the pin-outs, hold the regulator with its face towards you and legs pointing upward, the pin to the right is the input, middle pin is ground and left most pin is output.

B. Clock generator

A very simple astable multivibrator can be constructed using three inverters. It is known that the output of an inverter changes to the opposite state after a propagation delay when its input is changed. So, the signal at any point in this circuit changes state after a time equal to the sum of the propagation delays of the preceding gates and, therefore, a square wave is generated. It is possible to have some control over the frequency of the square wave by using timing elements such as resistors and capacitors.

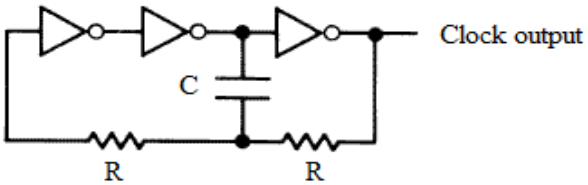

Fig. 3: Astable multivibrator using R and C as timing components

The figure shows a simple, reliable, and highly flexible astable circuit. In this case, the frequency of oscillation is determined primarily by the resistor and the capacitor timing components. Hence it is called an RC oscillator.

The exact relationship between the oscillation frequency and the R and C components depends in part on the electrical characteristics of the logic gates. For the standard TTL family of components, a resistance of approximately 400 Ω produces the relationship

$f = 1 / 0.001C$

Where, C is measured in µF and f in Hz. Thus to have a second pulse we have choose a capacitor of capacitance 1000 µF.

IC 7404, Hex-Inverter is used for the above purpose. Pin configuration of IC 7404 is as shown in Fig. 4.

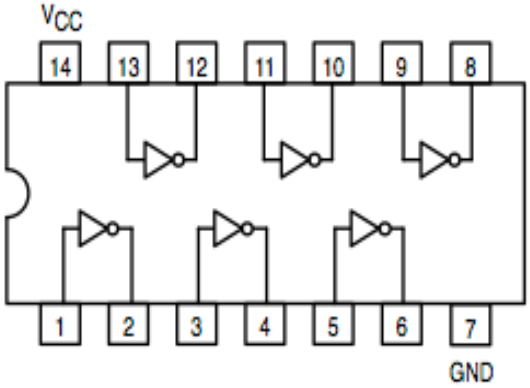

Fig. 4: IC 7404, Hex-Inverter

C. MOD-4 synchronous counter

The IC to be tested as well as multiplexer is to be supplied with series of $2^2 = 4$ combinations possible with two inputs. So, MOD-4 synchronous counter is used to do the same.

Considering the initial outputs as Q0=0 & Q1=0, whenever the first negative clock edge comes O/P of 1st FF becomes 1 as J & K for 1st FF is 1, the output of 1st FF toggles and changes from 0 to 1.

But when 1st cock edge had come output of 1st FF was 0. Hence J & K for 2nd FF for 1st edge are 0. So output of this FF doesn't change and we get Q1=0. So the output is $(Q1Q0)_2 = 01_2$.

On the next edge, output of 1st FF changes from 1 to 0 as J & K are always 1 for this FF. Inputs for 2nd edge for 2nd FF are J=1 & K=1. Hence output changes from 0 to 1. So we get the count as $(Q1Q0)_2 = 10_2$.

Similarly on the next edge we'll get the output count as $(Q1Q0)_2 = 11_2$.

And on the 4th clock edge both the outputs get reset and we get the output as $(Q1Q0)_2 = 00_2$ and again whole procedure is repeated.

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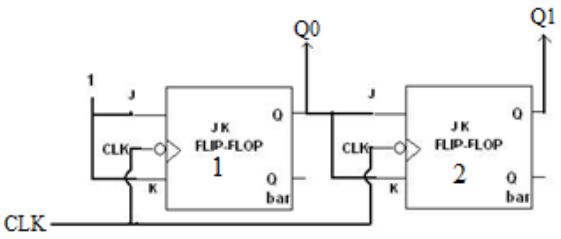

Fig. 5: Mod -4 Synchronous Up Counter

IC 7476, J-K flip-flop is used to construct Mod -4 synchronous up Counter. The pin configuration of IC 7476 is as shown in Fig. 6.

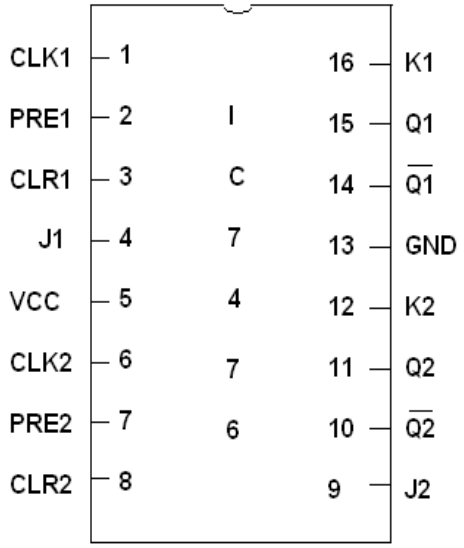

Fig. 6: Pin configuration of IC 7476

D. Output- generator

Instead of any microcontroller or any other memory unit, the output is generated instantly by a combinational circuit. A combinational circuit is designed to produce the outputs of various gates according to the inputs provided by the MOD-4 synchronous counter. A multiplexer can be used in place of logic gates to implement a logic expression. It can be so connected that it duplicates the logic of any truth table, i.e. it can generate any boolean algebraic function of a set of input variables. In such applications, the multiplexer can be viewed as a function generator, because it is easy to set or change the logic function it implements. One advantage of using a multiplexer in place of logic gates is that, a single integrated circuit can perform a function that might otherwise require numerous integrated circuits.

The first step in the design of a function generator using a multiplexer is to construct a truth table for the function to be implemented. Then, connect logic 1 to each data input of the multiplexer corresponding of the input variables the truth table shows the function to be equal to 1. Logic 0 is connected to the remaining data inputs. The variables themselves are connected to data select inputs of the multiplexer. The truth table for Y, implementation table and the logic diagram to implement Y using an 8:1 MUX are shown in the following figures.

TABLE 1 :TRUTH TABLE OF OUTPUT-GENERATOR

S0	S1	A	B	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	X
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X

The inputs S_0, A and B are applied to the data select inputs A, B, C respectively. Since Y=1 when S_0AB = 011, 101, 110, logic 1 is connected to data inputs D_3, D5and D_6. For S_0AB =001 and 010, Y= S_1. So D_1 and D_2 are connected to S_1. An extra inverter may be required if implemented in another way, which would increase the cost.

TABLE 2 IMPLEMENTATION TABLE

	S_0AB							
	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
S_1	000	001	010	011	100	101	110	111
0	0	1	2	**3**	8	**9**	**10**	11
1	4	**5**	**6**	**7**	12	**13**	**14**	15
	0	S_1	S_1	1	0	1	1	0

Logic 0 is connected to other data inputs D_0, D4 and D_7. These connections are shown in Fig. 8. IC 74151, an 8 channel digital Multiplexer is used for the above purpose.

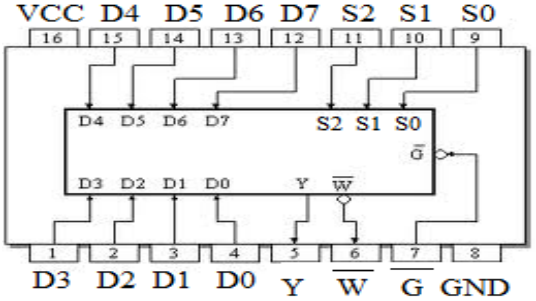

Fig. 7: Pin configuration of IC 74151

The present output Y is capable of producing the outputs of only AND, OR and EX-OR gates. To have outputs of other three i.e., NAND, NOR and EX-NOR, it is sufficient to

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complement the outputs of AND, OR and EX-OR gates respectively. But the complementary operation should be under control of some input, say S. On observing the truth tables of all the gates, EX-OR gate seems to be producing the B itself as output when A is '0' and complement of B when A is '1'. A and B refers to S (control input) and Y (MUX output) respectively. Thus the generation of all the required outputs is possible with the circuit shown below.

TABLE 3: TRUTH TABLE OF EX-OR GATE USED IN OUTPUT-GENERATOR

S	D
0	Y
1	Y'

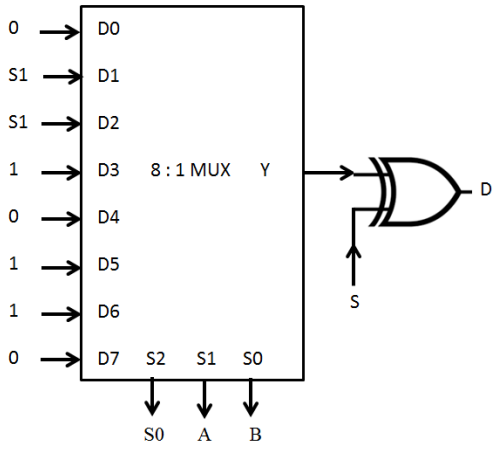

Fig. 8: Output generator

E. Test socket

Test socket is nothing but the IC base provided to place the IC that is to be tested. It is interfaced with the remaining circuits according to the circuit shown. A and B being the outputs of mod-4 synchronous up counter and Y1, Y2, Y3, Y4 being the outputs form IC, placed in test socket.

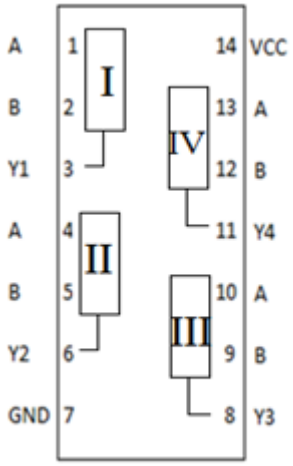

Fig. 9: Test socket

F. Inequality detector

To check the inequality between outputs from test socket and the correct output from output-generator, EX-OR gate is used. An EX-OR gate is a two input, one output logic circuit, whose output assumes a logic 1 state when one and only one of its two inputs assumes a logic one state. Since an X-OR gate produces an output 1 only when the inputs are not equal, it is called an anti-coincidence gate or inequality detector.

TABLE 4: TRUTH TABLE OF EX-OR GATE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Four EX-OR gates are required to compare output (D) of output-generator and outputs (Y1, Y2, Y3, Y4) of test socket.

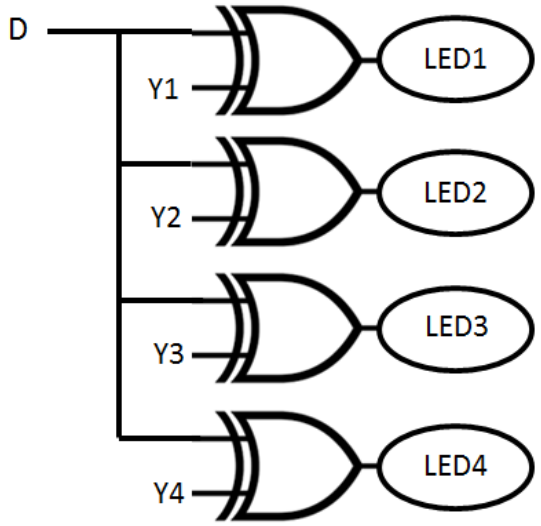

Fig. 10: Inequality detectors

The outputs of EX-OR gates is given to LEDs. Therefore, LEDs glow indicates the inequality. The fault in gates (labeled I, II, III, IV in Fig .9) of IC placed in test socket is indicated with corresponding LEDs (LED1, LED2, LED3, LED4) as shown in Fig.10.

There should be some circuit to indicate that the testing is completed. Usually, feeding the input "11" to output-generator and test socket by MOD-4 synchronous counter tends to the end of process. On observing the truth tables of all logic gates, AND gate alone outputs '1' for only input "11". So we have connected a buzzer to the output of the AND gate to indicate that the task of testing is completed.

V. TESTING PROCEDURE

The steps to be followed to test the IC are:

- Place the IC to be tested in the test socket
- Switch on the power supply
- Select the switches according to the function table shown below
- Observe the LEDs glow before the buzzer beeps out. LEDs glow indicates the fault.

The output was observed on the PDC Trainer Kit. The snapshot of the experimental setup made in the college laboratory to observe the result is shown in the Fig. 11.

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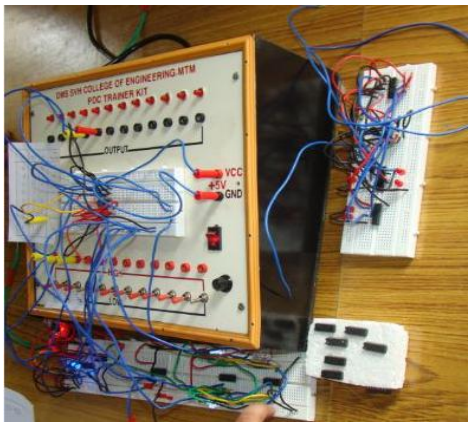

Fig. 11: Experimental setup on PDC Trainer Kit

TABLE 5: FUNCTION TABLE

S	S0	S1	Gate Enabled
0	0	0	AND
0	0	1	OR
0	1	0	EX-OR
0	1	1	-
1	0	0	NAND
1	0	1	NOR
1	1	0	EX-NOR
1	1	1	-

VI. COMPONENTS LIST

The components that are used to implement this digital IC tester are listed below.

TABLE 6: COMPONENTS LIST

S.No	Item	Specification	Quantity
1	Dual J-K Flip-Flop	IC 7476	1
2	8:1 Digital Multiplexer	IC 74152	1
3	Quad two-input EX-OR IC	IC 7486	2
4	Hex-Inverter	IC 7404	1
5	Transformer	12V	1
6	Resistors	390 Ω	2
7	Capacitors	220µF, 1000ΩF	1 each
8	Quad two-input AND IC	IC 7408	1
9	IC bases	14 pin 16 pin	5 2
10	Rectifier	D2SB	4
11	Three terminal voltage regulator IC	LM7805	1
12	LEDs		4+
13	Buzzer	1.5 V-12 V	1

VII. TECHNICAL SPECIFICATIONS

- FAMILY: TTL, CMOS
- RANGE: Logic Gates such as AND, OR, EX-OR, NAND, NOR and EX-NOR can be tested.
-
- TEST SOCKET: A single 14 pin socket for IC testing.
- PACKAGE**:** DIP 14 pins.
- FAIL INDICATOR: Bright LEDs.
- ELECTRICAL: 230 V (+/- 10 %), 1 phase, 50 Hz (+/- 2 %).
-

VIII. ADVANTAGES

- Reliable
- Less expensive
- Testing procedure is simple
-

IX. LIMITATIONS

- Only basic digital logic ICs can be tested
- Basic NOT gate cannot be tested
- Glitches are observed slightly
-

X. CONCLUSION

The model has been successfully designed at very low cost and so; it is best suitable for testing digital ICs in college laboratories. This would be more successful if it tests some more ICs.

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